AMENDMENTS TO THE ABSTRACT

Please amend the Abstract section of the specification as shown below in amendment form.

~~A data transmission system is provided comprising a disk controller and a read channel. The disk controller comprises a controller for controlling said first hardware component, a first clock for receiving a clock signal, a first transceiver for transmitting or receiving data, a first sync mark receiver to receive a sync mark signal, and a first data gate circuit for transmitting a data gate signal. The read channel comprises a second clock for transmitting the clock signal, a second transceiver for transmitting or receiving the data, a second sync mark transmitter transmitting the sync mark signal, and a second data gate circuit for receiving the data gate signal. During a read operation after the data gate signal is transmitted, the controller counts the clock signal when the sync mark is received and when the count is equal the amount of data to be read, a time period is dropped from the clock signal.~~

A system includes a read/write channel and a hard disk controller. The hard disk controller includes a latency-independent interface that communicates with the read/write channel. A serial control data circuit transmits a serial control data signal including serial control data, wherein the serial control data signal has a variable number m of words, wherein each of said m words comprises n bits, and wherein at least one of said n bits of each of said m words includes information indicating whether a subsequent word of said serial control data

signal will follow. A data circuit that transmits or receives data under the control of the serial control data signal.